What is claimed is:

1. A circuit for use with a multi-port memory device having an array of memory cells serviced by row decoders and column decoders, each cell being represented by a unique address;

an input/output control circuit for writing data into and reading data out of the array;

a first storage device for storing data to be input to said input/output control circuit;

a second storage device for storing address information;

and a control circuit for identifying which of a first and a second system may have access to the array and for generating signals for controlling the operation of said first and second storage devices and said input/output control circuit.

2. A circuit for transferring data between at least two ports and a single memory array, comprising:

an input/output control circuit for transferring data between the ports and the memory array;

a first storage device positioned between said input/output control circuit and the ports;

first and second row decoders, each responsive to addresses corresponding to data at one of the ports;

first and second column decoders, each responsive to addresses corresponding to data at one of the ports;

a second storage device for storing addresses to be input to said first and second row decoders and said first and second column decoders; and

a control circuit for producing signals for controlling the operation of said input/output control circuit and said first and second storage devices.

3. The circuit of claim 2 wherein said control circuit includes an arbitration circuit for identifying which of a first and a second system may have access to the array, and for producing signals for controlling the operation of said first and second storage devices so as to store the address and data from the system denied access to the array.

4. The circuit of claim 2 wherein said control circuit includes a mode select circuit for selecting a mode of operation, said mode defining the privileges which a first and a second system have with respect to the memory array.

5. A multi-port memory device responsive to two systems, comprising:

an array of memory cells;

first and second input/output ports;

an input/output control circuit responsive to said first and second input/output ports, said control circuit for writing data into and reading data out of said array;

first decoders responsive to the first system, said first decoders for producing first signals for accessing a cell within said array;

second decoders responsive to the second system, said second decoders for producing second signals for accessing a cell within said array;

a plurality of storage devices; and

a control circuit responsive to the first and second systems for identifying which of the systems is entitled to access to said array, and for controlling the operation of said input/output control circuit and said plurality of storage devices.

6. The memory device of claim 5 wherein the data is stored for a period of time sufficient to enable the system having access to complete its task.

7. The memory device of claim 5 wherein said control circuit includes an arbitration circuit having a first circuit for determining a valid access to an address in said array by one of the systems, a second circuit for detecting when an access is completed, and a third circuit responsive to said first circuit and said second circuit, said third circuit for generating a busy signal.

8. The memory device of claim 7 wherein said third circuit generates said busy signal when a valid access to an address is determined and ceases generation of said busy

signal when an end of cycle is detected for the system having access to said address.

9. The memory device of claim 8 wherein said third circuit includes a flip-flop.

10. The memory device of claim 5 wherein said control circuit includes a mode circuit responsive to mode control signals, said mode circuit for determining the degree of access to said array to which each of the two systems is entitled.

11. The memory device of claim 10 wherein said array of memory cells is divided into two sections, and wherein said mode control signals determine if both systems have read/write privileges to both said sections, if one system has read/write privileges to both said sections while said other system has read/write privileges to only one section of said array, and if one system has read/write privileges to one section of said array while the other system has read/write privileges to the other section of said array.

12. The memory device of claim 11 wherein said mode circuit includes a comparator circuit for determining the section specified in an address, a decoder circuit for decoding said mode control signals, and a logic circuit responsive to said comparator circuit and said decoder circuit for producing read and write control signals.

13. A multi-port memory device responsive to two systems, comprising:

an array of memory cells;

first and second input/output ports;

means, responsive to said first and second input/output ports, for writing data into and reading data out of said array;

first decoder means, responsive to the first system, for producing first signals for accessing a cell within said array;

second decoder means, responsive to the second system, for producing second signals for accessing a cell within said array;

a plurality of storage means; and

control circuit means responsive to the first and second systems for identifying which of the systems is entitled to access to said array, and for controlling the operation of said means for reading and writing and said plurality of storage devices.

14. A system comprising:

a first processor;

a second processor;

a first memory controller;

a second memory controller;

a plurality of multi-port memory devices each memory device comprising:

an array of memory cells each represented by a unique address;

first and second input/output ports;

an input/output control circuit responsive to said first and second input/output ports, said control circuit for writing data into and reading data out of said array;

a first storage device positioned between said first and second input/output ports and said input/output control circuit;

a first signal decoder circuit responsive to said first system for producing signals for accessing a cell within said array;

a second signal decoder circuit responsive to said second system for producing signals for accessing a cell within said array;

a second storage device for storing addresses; and

a control circuit responsive to said first and second systems for identifying which of the systems is entitled to access to said array and for controlling the operation of said input/output control circuit and said first and second storage devices;

a first bus connecting said first processor and said first memory controller;

a second bus connecting said first memory controller and said memory devices;

a third bus connecting said second processor and said second memory controller; and

a fourth bus connecting said second memory controller and said memory devices.

15. A method of operating a multi-port memory device of the type having an array of memory cells each represented by a unique row and column address, said multi-port memory device being responsive to two systems, said method comprising:

producing first signals for identifying an address of a cell within said array to which access is sought by the first system;

producing second signals for identifying an address of a cell within said array to which access is sought by the second system;

identifying which of the systems is entitled to access to said array in the event said first and second signals indicate both systems seek access to a same address at the same time; and

storing the address, and the data associated with said address, from the system not granted access.

16. The method of claim 15 wherein the data associated with said address from the system not granted access is stored for a period of time sufficient to enable the system having access to complete its task.

17. The method of claim 15 additionally comprising the steps of determining a valid access to an address in said array by one of the systems, detecting when an access is

completed, and generating a busy signal in response to said determining and detecting steps.

18. The method of claim 17 wherein said busy signal is generated when a valid access to an address is determined and ceases to be generated when an end of cycle is detected for the system having access to said address.

19. The method of claim 15 additionally comprising the step of determining the degree of access to said array to which each of the two systems is entitled.

20. The method of claim 19 wherein said array of memory cells is divided into two sections, and wherein said step of determining the degree of access includes determining if both systems have read/write privileges to both said sections, if one system has read/write privileges to both said sections while said other system has read/write privileges to only one section of said array, and if one system has read/write privileges to one section of said array while the other system has read/write privileges to the other section of said array.

21. The method of claim 20 wherein said step of determining the degree of access includes the steps of determining the section specified in an address, decoding said mode control signals, and producing read and write control signals in response to said determining and decoding steps.